

A High CMRR-CMOS Instrumentation Amplifier Intended for Bioimpedance Imaging

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ABSTRACT: The circuit is intended for a wideband bioimpedance imaging application. Front end amplifier required to have a high input impedance through which intended current is measured, signal coming from the tissue of human body is applied to a IA through electrodes, before going for a imaging. So that the signal can be boost up, detectable and immune to noise. For imaging of cancer biomarkers it is necessary to measure bioimpedance over a wide range of frequency 10 KHz to 2 MHz. This circuit provides 100 dB CMRR even at high frequency of 8 MHz, PSRR over 45 dB with good linearity, low power up to 567 microwatts. The IA occupies the area of 961 μm^2 . The benefits of using “current feedback” in instrumentation amplifier (IA) design are well known. When taking into account the differential gain response (25 to 40 dB), the average CMRR of the neutralized IA at 8 MHz exceeds 99 dB. Hence can be further used in various medical application like ECG, EIT etc.

KEYWORDS: Cancer biomarkers, CMOS, differential-mode gain, bioimpedance, high-frequency, high CMRR, instrumentation amplifier (IA), local current feedback, medical applications, wide bandwidth, imaging, Electrical Impedance Tomography (EIT), Electro Cardio Graph (ECG).

I. INTRODUCTION

An **instrumentation** (or **instrumentational**) **amplifier** is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. Instrumentation amplifiers are used where great accuracy and stability of the circuit both short and long-term are required.

These circuits find widespread use in nearly every medical device, both for the advantages previously mentioned and for the fact that instrumentation amplifiers are also precision gain devices. Instrumentation amps do not require external feedback resistors; instead they have laser-trimmed resistors fabricated onto the IC itself, using only a single external gain setting resistor to configure the amplification factor, eliminating resistor mismatches. This allows the device to have its gain set to an exact number, based on the needs of the circuit. Most biomedical sensors are very high impedance and generate tiny signals, such as blood pressure sensors, ultrasound transducers, polarized and non-polarized electrodes, and radiation thermometry transducers.

Application examples include automotive transducers [1], industrial process control[2]-[4], linear position sensing, and biopotential acquisition systems[6]-[11]. Main focus is on the design of integrated instrumentation for medical impedance imaging using bioimpedance measurements [12], [13]. Bioimpedance imaging is also known as electrical impedance tomography which is far better than the other medical imaging techniques. It has advantage over other techniques such as noise free, radiationless, highly portable, and inexpensive. In a bioimpedance imaging system a differential alternating current is applied through a pair of surface electrode to the body tissue and resulting voltages are picked up by another electrode which is further amplified and processed [15]. Amplifier has its necessity of high input impedance to avoid the part of produced current into the circuit, which would cause erroneous faults. Thus IA is required. The main focus is on to detect the microvolts (μvolts) differential signal of the body tissue in the presence of millivolts (mv) common mode interfering signal at working frequency of few Hz to MHz.

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Accurate Imaging requires a high CMRR in the range above 80 dB for the frequency up to 2-4 MHz[17]. For detecting such a low signal at high frequency a CMRR is required. CMRR is defined as the ratio of differential gain to common mode gain. Low power, low current consumption must be kept in mind while designing this IA with high 3dB frequency. Instrumentation amplifiers have uses in nearly every field of electronics; they fulfil a specific role in circuits needing the advantages of high input impedance with good gain while providing common mode noise rejection and fully differential inputs. This IA is designed using 180nm technology in cadence EDA tool with minimum area of 961 μm^2 .

II. RELATED WORK: SIMPLIFIED MODEL OF IA

Fig. 1 shows the simplified circuit schematic of the local current feedback IA[17]. The input transconductor stage uses a simple current mirror load (drain network) and current source biasing (source network). The sensing amplifier serves to exactly balance the drain currents of transistors M_{i1} and M_{i2} by adjusting the complementary currents I_1 and I_2 . A direct result of this is that the input differential voltage is forced across resistor R_1 and hence M_{i1} and M_{i2} of the input stage essentially acts as a unity-gain buffer. Similarly, the high gain amplifier B balances the drain currents of transistors M_{o1} and M_{o2} in the output transconductor stage. Since currents I_3 and I_4 are exact copies of I_1 and I_2 , respectively, the output voltage V_0 appears across resistor R_2 . Hence, the dc gain of the IA is given by the ratio R_2/R_1 . Placing a capacitor C_2 in parallel with resistor R_2 creates a dominant pole, which sets the 3 dB BW of the IA.

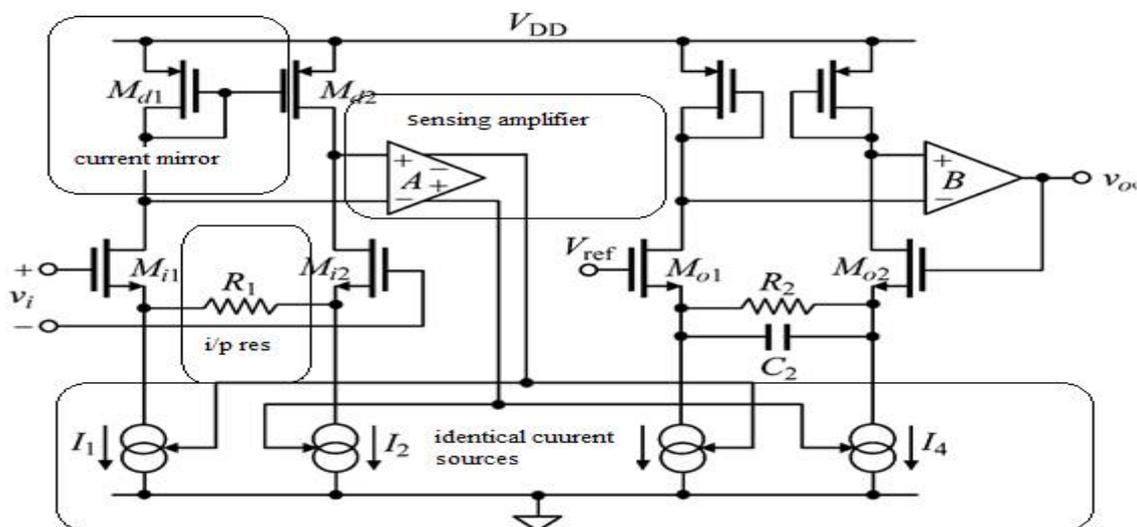


Fig. 1: Simplified model of a instrumentation amplifier with current feedback

The common-mode gain characteristics of the IA due to random mismatches can be analyzed by focusing only on the input stage. This is because the mismatch effects of the sensing amplifier A and the output transconductance stage are greatly suppressed by the high gain of the local feedback loops. Fig. 2 shows the small-signal model of the IA's input stage where it is assumed that the output conductances of $M_{d1, 2}$ are much less than their corresponding transconductances. The voltages at the drain terminals, d_1 and d_2 , are sensed by the amplifier A which drives the differential feedback current i_{fs} . The feedback path is via the source terminals s_1 and s_2 . In the figure, $g_{m1,2}$ and $g_{ds1,2}$ are respectively the transconductances and drain-source conductances of the input transistors M_{i1} and M_{i2} . $g_{md1,2}$ are the transconductances of the drain transistors M_{d1} and M_{d2} . $g_{s1,2}$ are the output conductances of the current sources I_1 and I_2 . All parasitic capacitances are included to allow a study of the high-frequency mismatch characteristics. $C_{s1,2}$ and $C_{d1,2}$ are respectively the gate-source and gate-drain capacitances of the input transistors

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Mi1 and Mi2, and Cs1,2 and Cd1,2 are respectively the *total* capacitances of the source and drain terminals, including those from the input and load/source transistors as well as the amplifier stages that are connected to the terminals.

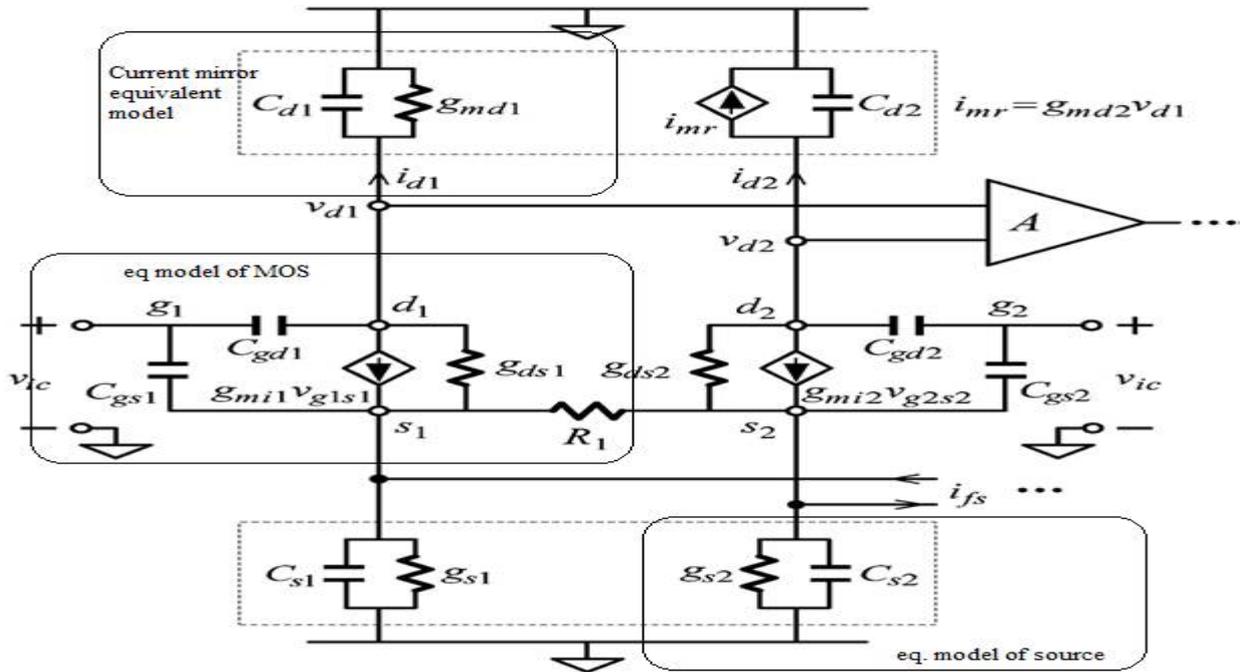


Fig. 2. IA input stage model for common-mode gain analysis

TABLE 1 Extracted small signal parameters of the designed IA

S.NO	CIRCUIT PARAMETER	TYPICAL VALUE	S.NO	CIRCUIT PARAMETER	TYPICAL VALUE
1.	R1/R2	400/20K ohms	5.	Gs	0.939 μS
2.	Gmi	543.7μS	6.	Cgs	2.43 PF
3.	Gds	0.546 μS	7.	Cgd	0.197 pF
4.	Gmd	145.5 μS	8.	Cgsd/Ced	0.217pF/2.07 pF
			9.	Cs	0.375 pF

Equations required for calculating common mode and differential gain:

On applying KCL equations at nodes s1, s2, d1, d2;

$$[SCs + Gs + Gmi - Gds + Gds] * Vs = [Gmi + SCgs] * Vic \dots\dots\dots eq(1)$$

$$[Gds + Gmi] * Vs - [Gmd - Gds - SCgd - SCd] * Vd = [Gmi - SCgd] * Vic \dots\dots\dots eq(2)$$

From eq(1) and (2) we get the two unknown and two equation, we can easily calculate Vd and Vs from here and hence common-mode gain.

$$(Gmi + 2/R1 + Gds + Gs + SCgs + SCs) * dVs/2 - Gds * (dVd/2) - Ifs = Gds * (Vd - Vs) - Gmi * (Vic - Vs) + Gs * Vs + SCgs * (Vic - Vs) + SCs * Vs \dots\dots\dots eq(3)$$

$$(Gmi + Gds) * dVs/2 - (Gds + SCgd + SCd) * dVd/2 - ifd = Gmi (Vic - Vs) + Gds (Vd - Vs) + Gmd * Vd - SCgd * (Vic - Vd) + SCd * Vd \dots\dots\dots eq(4)$$

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Hence from equation 3 and 4 we can easily calculate the differential gain.

In the ICF approach, the input common-mode voltage and reference common-mode voltage are independent of each other. This, however, comes at the price of an increased current dissipation. Therefore, the DCF approach is often used in biomedical low-power applications. This work focuses on gain accuracy and linearity, and therefore, the ICF approach is adopted.

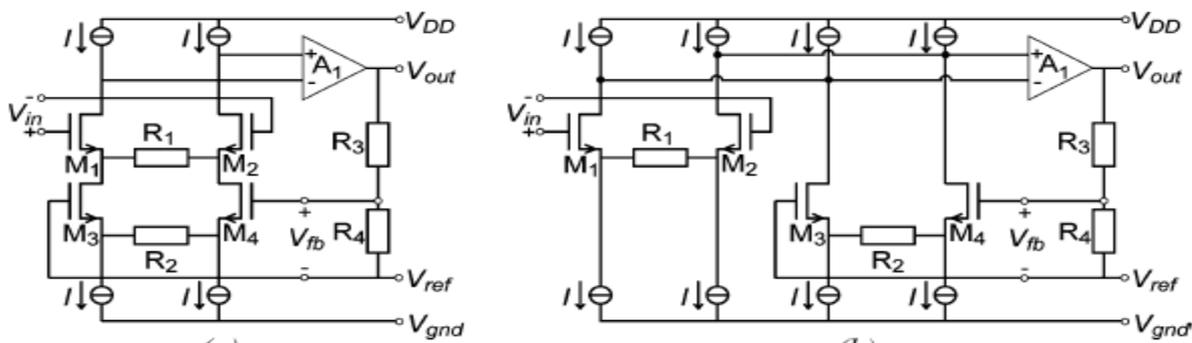


Fig 3: direct and indirect feedback loops IA [4]

III. PROPOSED WORK

Following is the schematic of the instrumentation amplifier with given specification, sizes of MOS, resistors, capacitors. It is designed in virtuoso design environment, using 180nm technology. Library files included is UMC18CMOS technology files, all the components are placed from the same library files. Three terminal resistors and capacitors are used and 3rd terminal is connected to VDD as body is of P-type. Total of 25 MOS with two resistors and 1 capacitor are required with a power supply of 1.8V.

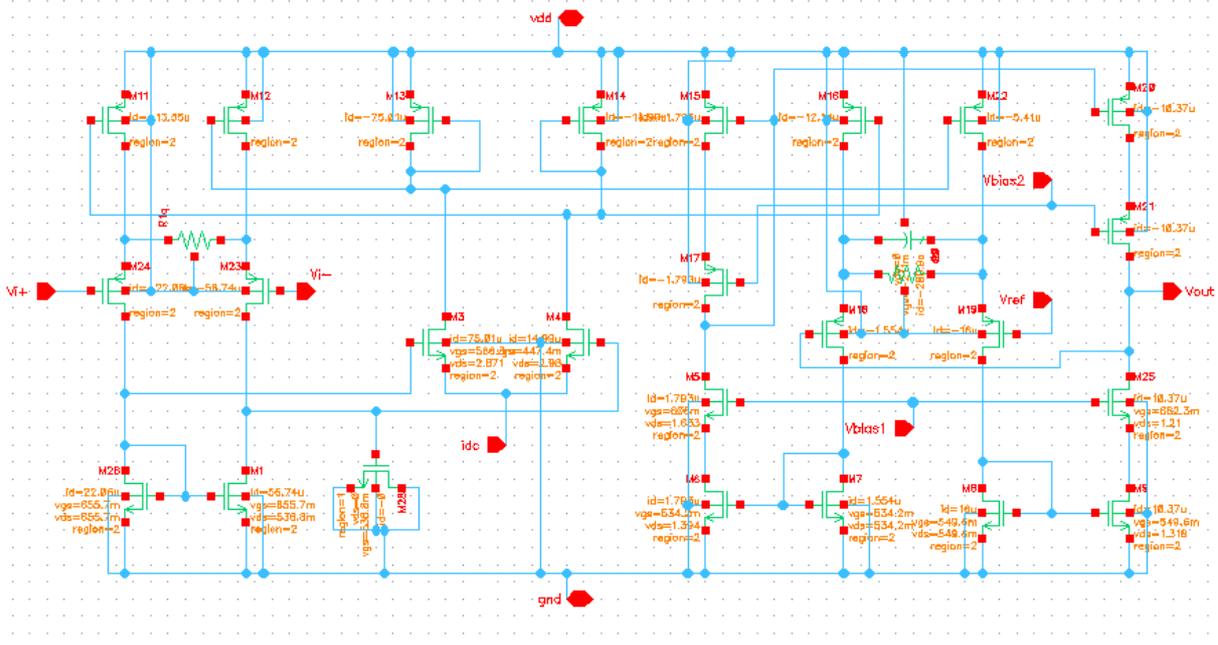


Fig 4: schematic diagram of an Instrumentation amplifier

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There are basically two approaches for designing of an IA. One is resistive feedback {3 opamp circuit of IA [11]} and second approach is current feedback [16]. Here we are using current feedback because of few reasons and disadvantages of resistive feedback circuits like CMRR is reduced by degree of matching of the resistors but in current feedback there is perfect isolation between input and output and balancing technique is also achieved.

In local current feedback IA there are few number of internal parasitic poles and thus this circuit offers a higher 3dB frequency and operating bandwidth. While in case of other feedback such as direct and indirect feedback [4] there are more number of poles associated with each stage and hence operating bandwidth reduces. Fig 1 current feedback is implemented with current mirror load transconductor [7]. One positive point of current mirror is insensitive to input offset voltage of loop amplifier. It also provides a large loop gain due to its higher impedance output node.

Ultimately sensing amplifier has relatively low gain and which will provide better stability, high bandwidth, hence power-area efficient.

IV. SIMULATED RESULTS OF IA

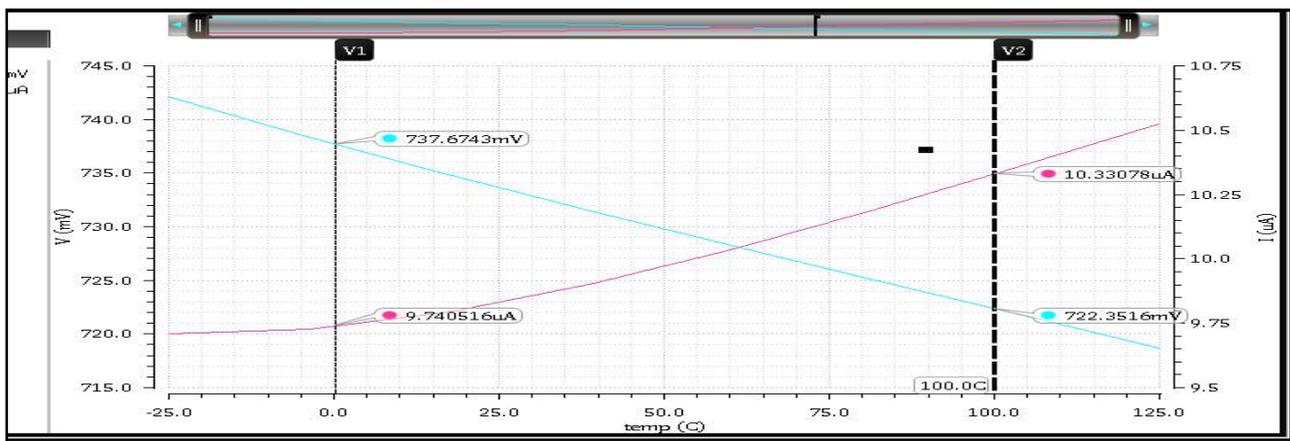


Fig 5: variation of Id(drain current) and output voltage with respect to temperature

Fig 5. Shows the output drain current and voltage relationship with temperature. As it is seen that current is increased from 9.74 μ A to 10.33 μ A only, even for 100 degree rise in temperature. Stability of the circuit is depends upon its current, voltage, and gain factor. Circuit should be able to work under tough conditions where the parameters like temp, pressure are playing major role. Here voltage is changes from 737mv to 722mv for the same temperature variation, which clearly shows the independency of temperature on this IA.

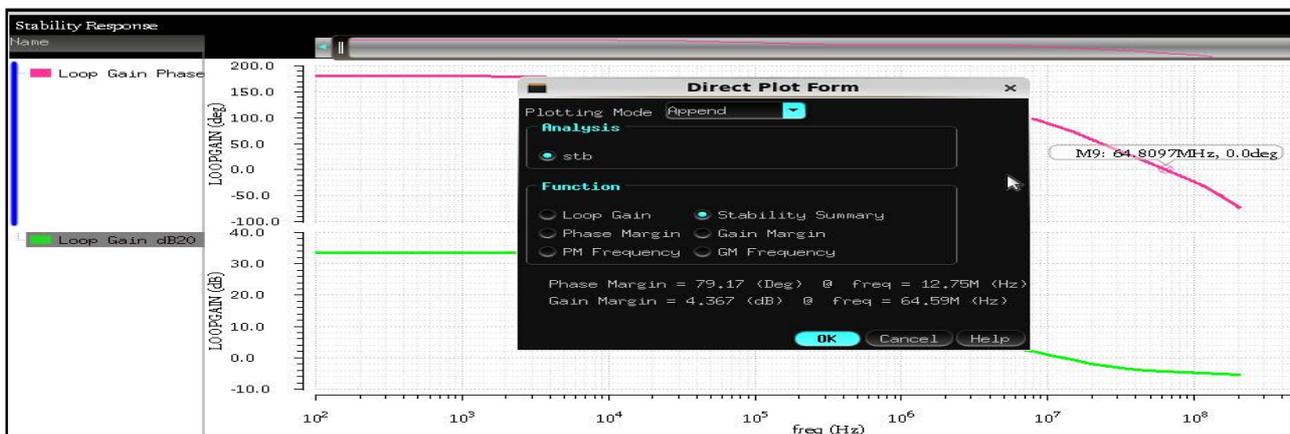


Fig 6: stability summary of simulated IA circuit

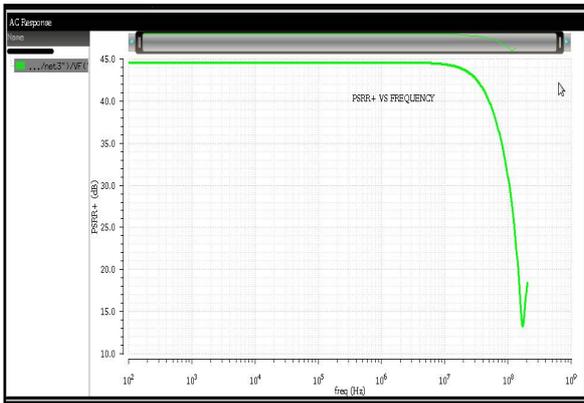


Fig 7: PSRR+ v/s frequency curve of IA

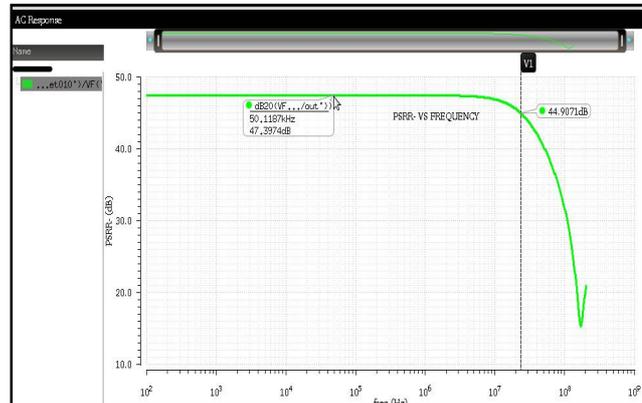


Fig 8: PSRR- v/s frequency curve of IA amplifier

Hence, gain of the IA would be the same as earlier one at higher temperature ranges also. This is a necessity of the circuit to be fabricated, which will provide better stability to the amplifiers that are going to work in noisy and tough conditions. Fig 6 shows the stability criterion in terms of frequency response, where gain margin and phase margin should be positive. Above 4dB of GM and for the PM of 79 degree the circuit will be stable. From the figure it can be concluded that $W_{pc} > W_{gc}$ and GM, PM are positive that indicates the system is stable enough, provided the loop gain should be high, MOSes operates in saturation region and bandwidth of the IA is enough for the requirement of operation. Fig 7 and 8 represents the PSRR+&- respectively which are more than 45 dB for both positive and negative supply. It is used to describe the amount of noise from a power supply that a particular device can reject. It can be defined as the ratio of the change in supply voltage in the IA to the equivalent output voltage it produces.

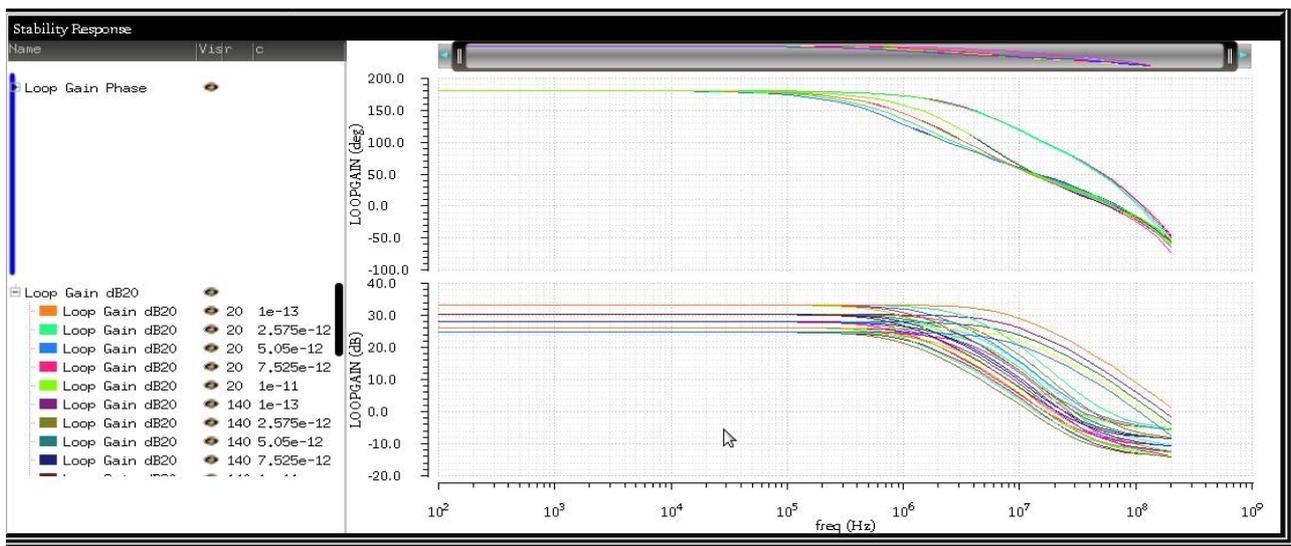


Fig 9: variation of gain v/s frequency with respect to different R1 (20 to 500 ohms) and C1 (1 to 10 pF)

Fig 9. Shows the variation of gain for the different values of resistor R1 (from 20 to 500 ohms with step size = 5) and capacitor C1 (from 1pF to 10 pF with step size of 5) and fixed output resistance at 20Kohms. So within this region the IA is stable i.e from 25 to 40 dB which is good enough for detecting the small signals. The above graph clearly shows for lower values of R1, the gain is more but we have to trade off between gain and stability here. Thus we cannot reduce R1 beyond 100 ohms.

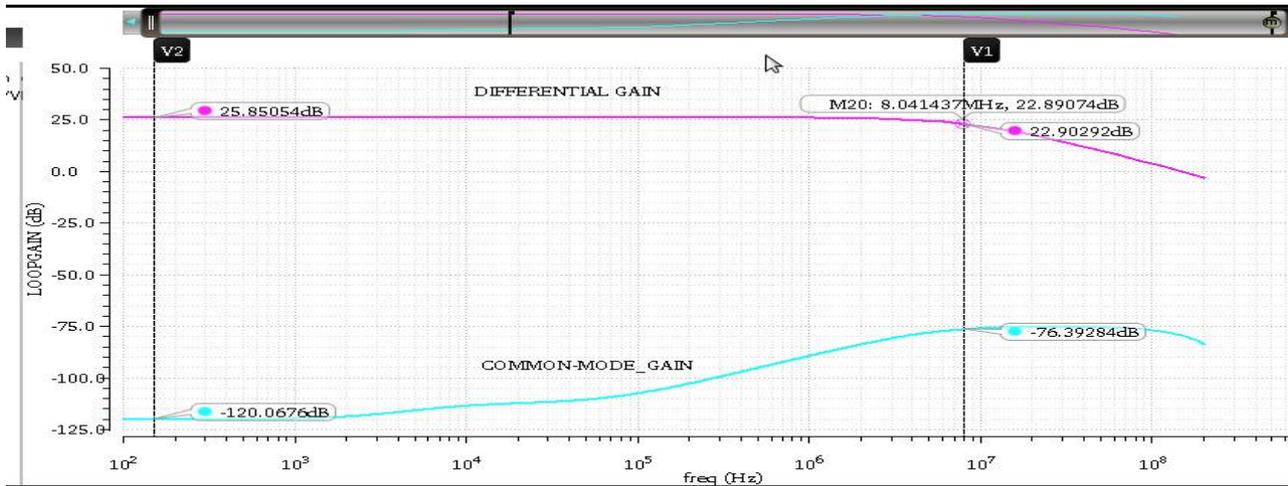


Fig 10: analysis of CMRR with Ad/Ac or Ad-(-Ac) in dB.

CMRR is defined as the ratio of differential gain to common mode gain. (CMRR = Ad/Ac), above figure shows Ad and Ac but they are in dB so we have to use logarithms identity rules here. Therefore $CMRR = Ad - [-Ac]$.

Calculating CMRR from fig 10 we get, CMRR at 8 MHz cut-off frequency = 22.90 - [-76.39]. Hence CMRR = 99.29 dB which is excellent at this frequency (which is our target result). At low frequency we are getting 145.85 dB and this is strong rejection to common mode noise. Detection of small signals from tissues in presence of high common mode signals is a challenging task and with this CMRR it is easily gettable.

The speed of the device should always be high enough to give quick response. Its slew rate should be infinite ideally. Slew rate is defined as the ratio of change in output voltage with respect to time. Here it is 38.3V/μS. Below is the layout of IA with minimum area and no DRC errors. Resistors are placed apart from power supply in order to achieve low mismatches and minimum resistive layers are used with proper design rules specifications.

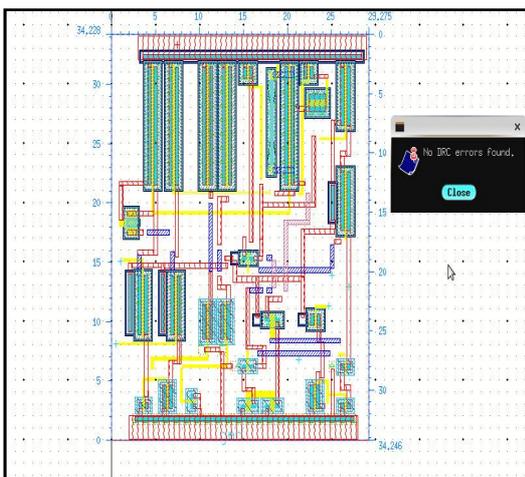


Fig 11: layout area of IA

S.NO	PARAMETERS	SPECIFICATIONS	RESULTS
1.	Process technology	-	180nm technology
2.	CMRR	>80 dB at 2MHz	100dB
3.	PSRR+	>40 dB at 2MHz	45 dB
4.	PSRR-	>40 dB at 2MHz	47 dB
5.	Differential gain	>30 dB	25-40 dB
6.	Common-mode gain	-	-76 dB at 8MHz
7.	Slew Rate	>2V/μS	38.3V/μS
8.	Area	Minimum as possible	961 μm-sq
9.	Power dissipation	<1mw	567μw
10.	Bandwidth	~2 to 10 MHz	8MHz
11.	Supply voltage	1.8V	1.8V
12.	Input referred noise	<20μV	9.8μV
13.	Gain Margin	Should be positive	4.3dB
14.	Phase Margin	Should be positive	79.17 deg
15.	Wgc	-	12.75MHz
16.	Wpc	-	64.59MHz

Table 2. Summary of simulation

For good linearity, the maximum differential input ranges is restricted to the value $2 * I_s * R_1$. Where current here is drain current of source transistor 22.04μA, voltage is therefore 2.2mv and above this harmonic distortion may occur. IIP3 analysis is also shown below fig 12 of 37.93dBm which is good enough. Hence high degree of linearity is obtained.

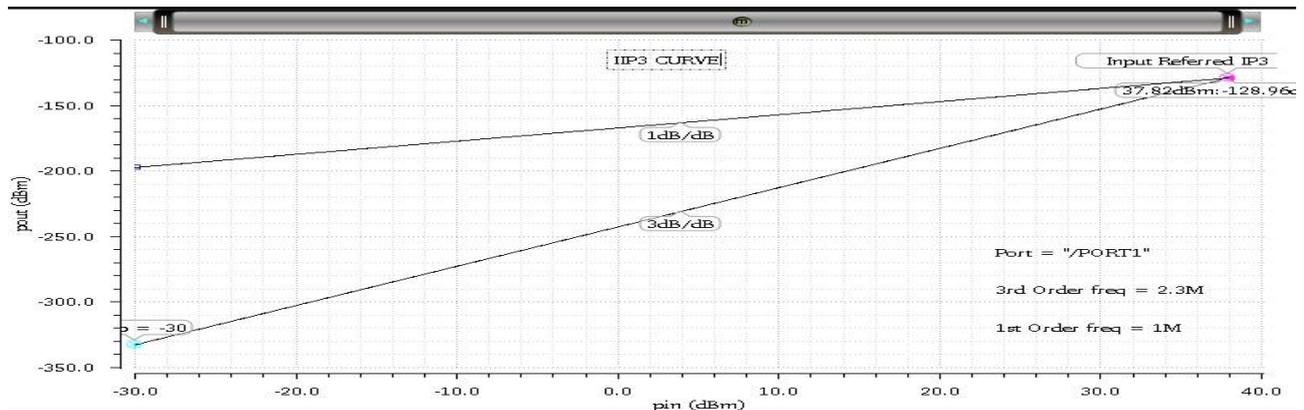


Fig 12. IIP3 analysis of IA

V. CONCLUSION AND FUTURE WORK

Instrumentation amplifiers are the basic building block of biomedical engineering. In order to achieve a better output from these micro inputs, an IA is the only option available. Whether it is industrial application or biomedical application it plays a major role in every stage of front end design. We are getting good CMRR at 8 MHz of 100 dB approximately and high slew rate, low dc power dissipation, good bandwidth, high stability with 4dB GM.

Future scope of this circuit is in implementation of IA for ECG application, by using a bandpass filter of low band we are able to get readings of heart tissues easily. Work is going on this application and it is a better option available.

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